10/542720

03 MAR 2004

Sertifikaat

REPUBLIC OF SOUTH AFRICA

PATENT KANTOOR
DEPARTEMENT VAN HANDEL
EN NYWERHEID

Rec'd PCT/PTO 20 JUL 2005

Certificate

REPUBLIEK VAN SUID-AFRIKA

PATENT OFFICE
DEPARTMENT OF TRADE AND
INDUSTRY

#2

Hiermee word gesertifiseer dat
This is to certify that

PCT/ZA04/00005

RECEIVED
23 MAR 2004
WIPO PCT

03 MAR 2004

1) South African Patent Application No. **2003/0552** accompanied by a Provisional specification was filed at the South African Patent Office on **21 January 2003** in the name of **Potchefstroom University for Christian Higher Education** in respect of an invention entitled: **"Insulated gate semiconductor device"**

2) The photocopy attached hereto is a true copy of the provisional specification and drawings filed with South African Patent Application No. **2003/0552.**

Geteken te **PRETORIA** in die Republiek van Suid-Afrika, hierdie 23th dag van February 2004

Signed at **PRETORIA** in the Republic of South Africa, this 23th day of February 2004

Registrar of Patents

PRIORITY DOCUMENT
SUBMITTED OR TRANSMITTED IN COMPLIANCE WITH RULE 17.1(a) OR (b)

BEST AVAILABLE COPY

REPUBLIC OF SOUTH AFRICA

Form P.2

PATENTS ACT, 1978

REGISTER OF PATENTS

OFFICIAL APPLICATION NO.	LODGING DATE : PROVISIONAL	ACCEPTANCE DATE
21 01 2003/0552	22 21 January 2003	43
INTERNATIONAL CLASSIFICATION	**LODGING DATE : COMPLETE**	**GRANTED DATE**
51	23	

FULL NAME(S) OF APPLICANT(S) / PATENTEE(S)

71 POTCHEFSTROOM UNIVERSITY FOR CHRISTIAN HIGHER EDUCATION

APPLICANTS SUBSTITUTED :	DATE REGISTERED
71	

ASSIGNEE(S)	DATE REGISTERED
71	

FULL NAME(S) OF INVENTOR(S)

72 VISSER, Barend

DE JAGER, Ocker, Cornelis

PRIORITY CLAIMED	COUNTRY	NUMBER	DATE
N.B. Use international abbreviation for country. (See Schedule 4)	33	31	32

TITLE OF INVENTION

54 INSULATED GATE SEMICONDUCTOR DEVICE

ADDRESS OF APPLICANT(S) / PATENTEE(S)

1 Hoffman Street
Joon van Rooy Building
Potchefstroom
2531
South Africa

ADDRESS FOR SERVICE

74 D M Kisch Inc, 54 Wierda Road West, Wierda Valley, SANDTON

REF P26067ZA00

PATENT OF ADDITION NO.	DATE OF ANY CHANGE
61	

FRESH APPLICATION BASED ON	DATE OF ANY CHANGE

REPUBLIC OF SOUTH AFRICA
PATENTS ACT, 1978

REVENUE PAID 21.1.03 INKOMSTE BETAAL

REPUBLIC OF SOUTH AFRICA
R 6 0.0 0
REPUBLIEK VAN SUID-AFRIKA

PBHR 229

APPLICATION FOR A PATENT AND ACKNOWLEDGEMENT OF RECEIPT
(Section 30 (1) - Regulation 22)
The grant of a patent is hereby requested by the undermentioned applicant on the basis of the present application filed in duplicate.

OFFICIAL APPLICATION NO	
21	01 2003/0552

DMK REFERENCE
P26067ZA00

FULL NAME(S) OF APPLICANT(S)

71 POTCHEFSTROOM UNIVERSITY FOR CHRISTIAN HIGHER EDUCATION

ADDRESS(ES) OF APPLICANT(S)

1 Hoffman Street
Joon van Rooy Building
Potchefstroom
2531
South Africa

TITLE OF INVENTION

54 INSULATED GATE SEMICONDUCTOR DEVICE

THE APPLICANT CLAIMS PRIORITY AS SET OUT ON THE ACCOMPANING FORM P2
The earliest priority claimed is

THIS APPLICATION IS FOR A PATENT OF ADDITION TO PATENT APPLICATION NO.	21	01	
THIS APPLICATION IS FRESH APPLICATION IN TERMS OF SECTION 37 AND BASED ON APPLICATION NO.	21	01	

THIS APPLICATION IS ACCOMPANIED BY :

x	1a	A single copy of a provisional specification of 16 pages.
	1b	Two copies of a complete specification of pages.
	2a	Informal drawings of sheets.
x	2b	Formal drawings of 8 sheets.
	3	Publication particulars and abstract (form P8 in duplicate).
	4	A copy of figure of the drawings for the abstract.
	5	Assignment of invention (from the inventors) or other evidence of title.
	6	Certfied priority document(s).
	7	Translation of priority document(s).
	8	Assignment of priority rights.
	9	A copy of form P2 and a specification of S.A. Patent Application. 21 01
	10	A declaration and power of attorney on form P3.
	11	Request for ante-dating on form P4.
	12	Request for classification on form P9.
	13a	Request for delay of acceptance on form P4.
	13b	

DATED 21 January 2003

Patent Attorney(s) for Applicant(s)

ADDRESS FOR SERVICE

74 D M Kisch Inc
Inanda Greens Business Park
54 Wierda Road West
Wierda Valley
SANDTON

RECEIVED
OFFICIAL DATE STAMP 2003-01-21

REGISTRAR OF PATENTS DESIGNS, TRADE MARKS COPYRIGHT
REGISTRATEUR VAN PATENTE, MODELLE, HANDELSMERKE EN OUTEURSREG

The duplicate will be returned to the applicant's address for service as proof of lodging but is not valid unless endorsed with official stamp.

D. M. Kisch Inc, Sandton

Form P.6

REPUBLIC OF SOUTH AFRICA

PATENTS ACT, 1978

PROVISIONAL SPECIFICATION

(Section 30 (1) - Regulation 27)

OFFICIAL APPLICATION NO.	LODGING DATE	DMK REFERENCE
21 2003/0552	22 21 January 2003	P26067ZA00

FULL NAME(S) OF APPLICANT(S)

71 POTCHEFSTROOM UNIVERSITY FOR CHRISTIAN HIGHER EDUCATION

FULL NAME(S) OF INVENTOR(S)

72 VISSER, Barend

DE JAGER, Ocker, Cornelis

TITLE OF INVENTION

54 INSULATED GATE SEMICONDUCTOR DEVICE

INTRODUCTION AND BACKGROUND

THIS invention relates to insulated gate semiconductor devices such as metal oxide silicon field effect transistors (MOSFET's), more particularly to such devices for use in switching applications and to a method of driving such devices.

BACKGROUND ART

Capacitance inherent in the gate structures of insulated gate devices limits the switching speeds of these devices. It is also well known that the Miller effect has an influence on the capacitance at the gate of devices of the aforementioned kind.

In known MOSFET structures, it is presently preferred to minimize the gate voltage V_{GS} required for switching of the device and which then implies a relatively large input gate capacitance. The total switching time T_s of the device is constituted by the sum of a turn-on delay time T_{don} and a rise time T_r or fall time T_f.

It is further known that due to the Miller effect an input capacitance of a typical commercially available MOSFET varies during switching of the device. The capacitance has a first value C_{iiss} when the device is off and a second value C_{fiss} when the device is on. The ratio of the second and first values for a known and commercially available IRF 740

MOSFET is in the order of 2.5. It has been found that such a ratio impairs the switching speed of these devices.

The total switching time T_s of an IRF 740 MOSFET to switch on is made up by the sum of a turn-on delay time T_{don} of 14ns and a drain source voltage fall time T_f of about 24ns and is equal to about 38ns. The corresponding time to switch off is about 77ns. These times are too long for some applications.

OBJECT OF THE INVENTION

Accordingly, it is an object of the present invention to provide an insulated gate device and method of driving such a device with which the applicant believes the aforementioned disadvantages may at least be alleviated.

SUMMARY OF THE INVENTION

In this specification the term "Miller parameter" (β) is used to denote a product of a constant and the difference between an inverse of a first value of a gate capacitance of an insulated gate device, that is when the device is off and an inverse of a second value of the gate capacitance, that is when the device is on. That is:

$$\beta \approx A(1/C_{iiss} - 1/C_{fiss})$$

According to one aspect of the invention there is provided an insulated gate device comprising a gate and an insulation layer at the gate, the layer having a thickness (d) of at least a quotient of a Miller parameter as defined and a ratio of maximum charge accommodatable on the gate and a minimum charge required on the gate for complete switching, minus one (1). That is:

$$d \geq d_{min} \approx \beta / \left[\left(Q_{G(max)} / Q_{G(min)} \right) - 1 \right]$$

where $Q_{G(max)}$ is the maximum allowable steady state charge for safe operation and $Q_{G(min)}$ is the minimum charge required for complete switching. The aforementioned charge values are independent of d and may be derived from state-of-the-art technology.

According to another aspect of the invention there is provided an insulated gate device comprising a gate, the device having a capacitance at the gate which is a function of the thickness of an insulation layer at the gate, the thickness of the layer being selected to ensure that a first ratio between a final value of the capacitance when the device is on and an initial value of the capacitance when the device is off is smaller or equal to a second ratio of a maximum charge receivable on the gate and a charge required to reach a threshold voltage of the gate of the device.

According to yet another aspect of the invention there is provided an insulated gate device comprising a gate, the device having a capacitance at the gate which is a function of the thickness of an insulation layer at the gate, the thickness of the layer being selected to ensure that a first ratio between a final value of the capacitance when the device is on and an initial value of the capacitance when the device is off is smaller or equal to a second ratio of a maximum voltage applyable to the gate and a threshold voltage required on the gate to switch the device on.

According to still anther aspect of the invention there is provided an insulated gate device comprising a gate, the device having a capacitance at the gate which is a function of the thickness of an insulation layer at the gate, the thickness being such that a ratio between a final value of the capacitance when the device is on and an initial value of the capacitance when the device is off is smaller than 2.5.

The first ratio is typically less than 2, preferably less than 1.5, more preferably less than 1.4, even more preferably less than 1.3, still more preferably less than 1.2 and most preferably less than 1.1.

According to yet another aspect of the invention there is provided a method of driving an insulated gate semiconductor device, the device comprising an insulation layer at a gate thereof providing a capacitance which varies between an initial value when the device is off and a final value when the device is on, the method comprising the step of depositing at least a Miller charge on the gate while the capacitance has said initial value.

The method preferably comprises the step of depositing substantially sufficient charge for a desired steady state switched on state of the device on the gate while the capacitance has said initial value.

The device may be a semiconductor device.

The device may be a field effect transistor (FET), preferably a metal oxide silicon field effect transistor (MOSFET).

BRIEF DESCRIPTION OF THE ACCOMPANYING DIAGRAMS

The invention will now further be described, by way of example only, with reference to the accompanying diagrams wherein:

figure 1 is a diagrammatic representation of a known insulated gate semiconductor device in the form of a MOSFET;

figure 2(a) is a diagrammatic representation of a gate structure of the MOSFET while it is off;

figure 2(b) is a diagrammatic representation of a gate structure of the MOSFET when it is partially on;

figure 2(c) is a diagrammatic representation of a gate structure of the MOSFET when it is fully switched on;

figure 3 is a typical graph for the steady state of gate-to-source voltage against total gate charge marked A of a conventional MOSFET as well as various similar graphs marked B for MOSFET's according to the invention;

figure 4 is a graph of total switching time against a ratio of initial charge transferred to the gate and the Miller charge of a variety of MOSFET's;

figure 5 is a graph of drain-source rise time against turn-on delay time of a variety of MOSFET's;

figure 6 is a graph of minimum and maximum gate source voltages required on a MOSFET according to the invention against total switching time;

figure 7(a) are oscillographs of V_{GS} and V_{DS} against time for a MOSFET with a ratio $C_{fiss}/C_{iiss} \approx 2.16$;

figure 7(b) are similar graphs for a MOSFET with a ratio $C_{fiss}/C_{iiss} \approx 1.62$;

figure 7(c) are similar graphs for a MOSFET with a ratio $C_{fiss}/C_{iiss} \approx 1.34$; and

figure 7(d) are similar graphs for a MOSFET with the ratio $C_{fiss}/C_{iiss} \approx 1.17$.

DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

An insulated gate semiconductor device in the form of a known metal oxide silicon field effect transistor (MOSFET) is generally depicted by the reference numeral 10 in figure 1.

The MOSFET 10 comprises a gate 12, a drain 14 and a source 16. The device 10 has a gate capacitance C_g between the gate and the source.

It is well known that when a voltage V_{GS} is applied to the gate as shown at 80 in figure 7(a), charge is deposited on the gate causing the device to switch on and a voltage V_{DS} to switch from a maximum value shown at 82 to a minimum value shown at 84. Similarly, when the charge is removed from the gate, the device is switched off and the voltage V_{DS} switches to the maximum value.

The total switching time T_s is constituted by the sum of a turn-on delay time T_{don} and a rise time T_r. The turn-on delay time is defined to be the time between rise of the gate-to-source voltage V_{GS} above 10% of its maximum value and the onset of drain-to-source conduction, that is when the voltage V_{DS} has decreased by 10%. The rise time is defined

as the time interval corresponding to a decrease in V_{DS} from 90% to 10% of its maximum value when the device is switched on.

If a gate voltage, V_{GS}, substantially larger than the threshold gate voltage, V_{GST}, is supplied in a time much shorter than the turn-on delay time, the latter may be approximated as

$$T_{don} \quad (2\pi/3)\ (L_S\, C_{iiss})^{1/2}$$

Referring to figures 2(a) to 2(c), in the known devices, the gate capacitance C_G may be modelled as effectively comprising two capacitors C_g and C_c in series. As shown in figures 2(a) to 2(c) the first capacitor C_g is an invariable capacitor and its value scales to 1/d, being the thickness (d) of an insulation layer 18 at the gate of the device. The second capacitor C_c is a variable capacitor having a value of ∞ when the device is switched on as shown in figure 2(c) and a value of $1/\alpha$ when the device is off as shown in figure 2(a). The gate capacitance C_G may hence be written as:

$$C_G = 1/[1/C_g(d) + 1/C_c(\alpha)]$$
$$= A/(d+\alpha)$$

where A is an effective area, which includes proper normalization constants. Thus, α is a maximum when the device is switched off as shown in figure 2(a) and $\alpha = 0$ when the device is switched on as shown in figure 2(c).

A Miller parameter (β) which is proportional to a difference in the inverse of the gate capacitances when the device is off C_{ilss} and when the device is on C_{fiss} is defined as follows:

$$\beta \approx A(1/C_{ilss} - 1/C_{fiss}).$$

The ratio C_{fiss} / C_{ilss} may be written as $(d+\alpha)/d$.

According to the invention by increasing the thickness d of the layer 18 and hence by decreasing the gate capacitance C_G, the total switching time T_s of a MOSFET 10 may be decreased. A minimum value for thickness d is given by:

$$d \geq \beta / \left[\left(Q_{G(max)} / Q_{G(min)} \right) - 1 \right]$$

wherein $Q_{G(min)}$ is the minimum charge required for complete switching and wherein $Q_{G(max)}$ is the maximum allowable gate charge on the device, before damage to the device.

Defining $V_{GS(min)}$ as the minimum gate (12) voltage for complete switching and $V_{GS(max)}$ as the maximum allowable gate voltage on the device, before damage to the device, it is known that $Q_{G(max)} / Q_{G(min)} > V_{GS(max)} / V_{GS(min)}$. This inequality implies a slightly larger limit than that calculated from the charge ratios $Q_{G(max)} / Q_{G(min)}$:

$$d \geq \beta / \left[\left(V_{GS(max)} / V_{GS(min)} \right) - 1 \right]$$

With this minimum thickness for d, the switching time of the device is mainly limited by the gate source inductance and capacitance. By increasing d beyond this minimum, allows for reducing the rise or fall time by compensating for the source inductance L_s voltage ε_s during switching and which is:

$$\varepsilon_s = L_s \, di/dt + iR_s$$

$$\varepsilon_{s(max)} \approx L_s \, I_{DS(max)} / T_s + I_{DS(max)} \, R_s.$$

It can be shown that:

$$T_s \; \alpha \; 1/d^{½}$$

which indicates that the total switching time is reduced by increasing the thickness d of layer 18. The minimum required voltage to switch the device will also increase as will become clear hereinafter.

In Table 1 there are provided relevant details of four different MOSFET's with progressively increasing thickness d of the insulation layer 18 and hence progressively decreasing gate capacitance, C_G.

Table 1

No.	Modified Input Gate Capacitance C_{iiss}, C_{fiss} (nF)	Applied Gate Voltage V_{GS} (volt)	Initial & Final Gate Charge Transferred $C_{iiss}V_{GS}$ & $C_{fiss}V_{GS}$ (nC)	Turn-on Delay Time Predicted & Observed $T_{d(on)}$ (ns)	**Measured Switching Time** T_s (ns)
i	1.2 2.6	15	18 40	6.3 6 (20 ns/div)	**38**
ii	0.86 1.4	32	28 45	5.3 5 (20 ns/div)	**20**
iii	0.58 0.78	120	70 94	4.4 <2 (10 ns/div)	<4
iv	0.35 0.41	200	70 82	3.4 < 2 (10 ns/div)	<4

For a conventional IRF 740 MOSFET:

$$\varepsilon_{s(max)} \approx 7.4 \text{ nH (40 A/27 ns)} + 4 \text{ volt} = 15 \text{ volt}$$

$$V_{G(internal)} \approx V_{GS(max)} - \varepsilon_{s(max)} = 20 \text{ volt} - 15 \text{ volt} = 5 \text{ volt}$$

For the device in row iv of Table 1

$$\varepsilon_{s(max)} \approx 7.4 \text{ nH (40 A/2.5 ns)} + 5 \text{ volt} = 123 \text{ volt}$$

$$V_{G(internal)} \approx V_{GS(max)} - \varepsilon_{s(max)} \approx 200 \text{ volt} - 123 \text{ volt} = 77 \text{ volt}$$

From this example it is clear that $V_{G(internal)}$ is still larger than the modified threshold gate voltage $V_{GSTM} = V_{GS(min)} = 73$ volt, shown in figure 3, and the slow rise time due to the Miller effect is this

effectively counteracted. It follows that minimization of the product $L_S C_{iiss}$ minimizes the switching time T_S of the device.

Another important feature of the invention is that at least a minimum required charge $Q_{G(min)}$ or Miller charge (see figure 3) must be transferred to the gate while the gate capacitance assumes its lower initial value of C_{iiss} rather when the larger input capacitance C_{fiss} determines the final switched state of the MOSFET. Hence the charge to be transferred is

$$Q_G = V_{GS} C_{iiss} \geq Q_{G(min)}.$$

Thus, the following minimum source to gate voltage must be applied.

$$V_{GS} \geq V_{GS}(min) = Q_{G(min)}/C_{iiss},$$

Also,

$$Q_G = V_{GS} C_{fiss} \leq Q_{G(max)}$$

and the corresponding voltage limit is given by

$$V_{GS} \leq V_{GS(max)} = Q_{G(max)} / C_{fiss}$$

This could also be written as:

$$C_{fiss} / C_{iiss} \leq Q_{G(max)} / Q_{G(min)}$$

or

$$C_{fiss} / C_{iiss} \leq V_{GS(max)} / V_{GS(min)}$$

Oscillograms illustrating V_{GS} and V_{DS} against time during switching on for each of the devices referenced i to iv in Table 1 are shown in figures 7(a) to 7(d) respectively. The decrease in gate capacitance is clear from the second column in the Table, and the larger required input V_{GS} and decreasing switching times are clear from both the Table and the oscillograms.

The last two devices iii and iv in Table 1 with minimized gate capacitance and wherein the ratio $C_{fiss}/ C_{iiss} < 1,34$, represent MOSFET's close to optimum, since the initial gate charge is already more than the minimum gate charge $Q_{G(min)}$ (shown in figure 3 and which for a typical MOSFET is in the order of 30nC) required for complete switching. The increased gate to source input voltage V_{GS} and spectacular drop in total switching times T_s are noticeable.

In figure 3, comparative graphs for a known MOSFET is shown at A and for a MOSFET's according to the invention at B. The ratio C_{fiss}/C_{iiss} for the known IRF 740 MOSFET is in the order of 2.5 whereas the same ratio for the last device according to the invention in Table 1 is 1.17. The device according to the invention has a total switching time of < 4ns which is about an order faster than the 38ns of the known and comparable IRF 740 MOSFET.

In figure 4 there is shown a graph of total switching time as a function of the initial gate charge relative to the minimum gate charge $Q_{G(min)}$. The circle at 40 represent standard operation of an IRF 740 MOSFET. However, the circles at 42 and 44 illustrate the improved operation of the MOSFET's referenced iii and iv in Table 1.

In figure 5 there is shown a graph of rise time T_r against turn-on delay time T_{don} for a plurality of different devices. The circle at 50 indicates standard operation of an IRF 740 MOSFET and the circles 52 and 54 indicate the improvement in total switching time T_S of the devices referenced iii and iv in Table 1 to a point where the rise time becomes negligible and the total switching time T_S approximates the turn-on delay time T_{don}.

It can further be shown that the product of V_{GS} and the square of the total switching time T_S is band limited as follows:

$$(2\pi/3)^2 \, Q_{G(min)} \, L_S \qquad V_{GS} T_S^2 \qquad (2\pi/3)^2 \, Q_{G(max)} \, L_S$$

which means that the operating voltage V_{GS} of the device according to the invention (which is much higher than the corresponding voltage for prior art devices) is limited as follows:

$$(2\pi/3)^2 \, Q_{G(min)} \frac{L_S}{T_S^2} \qquad V_{GS} \qquad (2\pi/3)^2 \, Q_{G(max)} \frac{L_S}{T_S^2}$$

and as illustrated in figure 6. The internal source resistance R_S has a negligible effect on these expressions and is therefore omitted for better clarity.

Hence, by minimizing the product of Miller charge or $Q_{G(min)}$ and L_S, reduced total switching times T_S and required operating voltages V_{GS} may be achieved.

It will be appreciated that there are many variations in detail on the device and method according to the invention, without departing from the scope and spirit of this disclosure.

Dated this 21 day of January 2003

Patent Attorney / Agent for the Applicant

POTCHEFSTROOM UNIVERSITY FOR CHRISTIAN
HIGHER EDUCATION

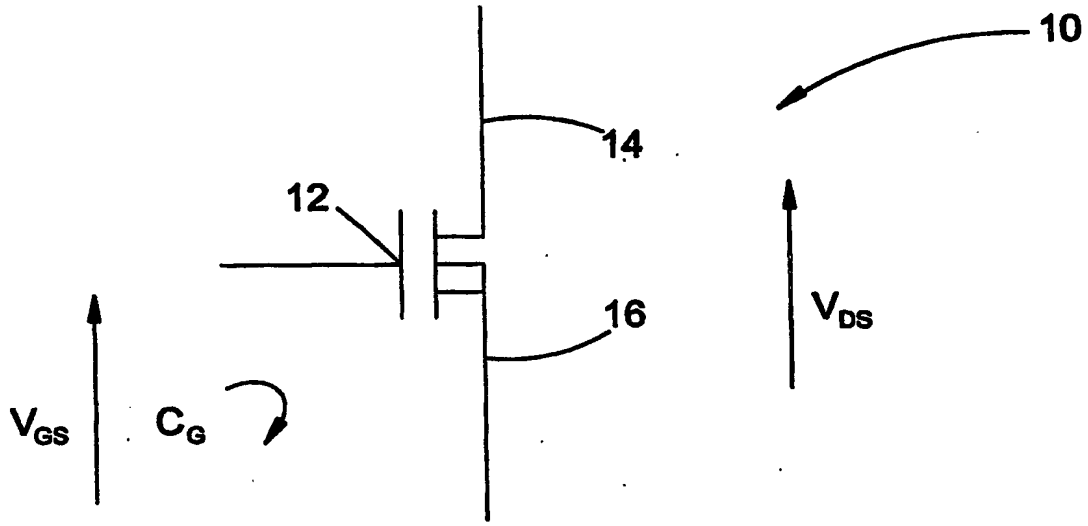

FIGURE 1

D.M. KISCH INC.
Patent Attorneys
JOHANNESBURG

Patent Attorney for the Applicant

POTCHEFSTROOM UNIVERSITY FOR CHRISTIAN HIGHER EDUCATION

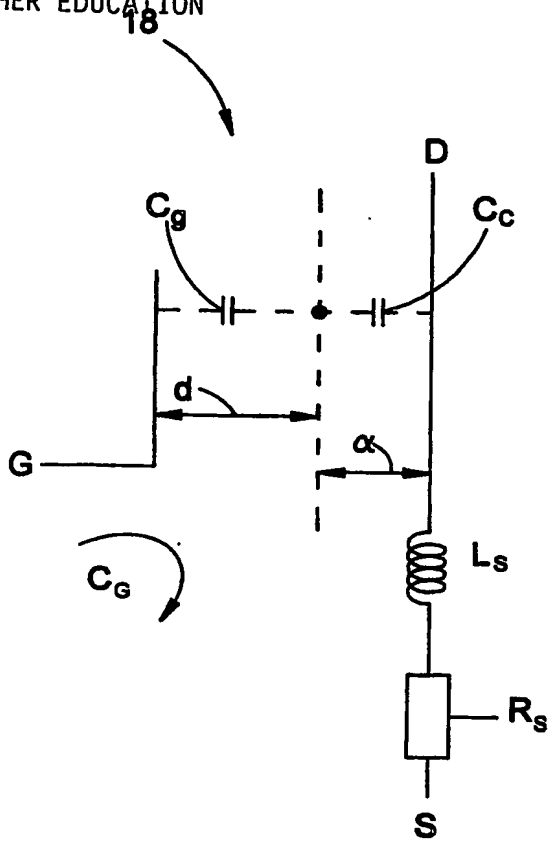

FIGURE 2(a)

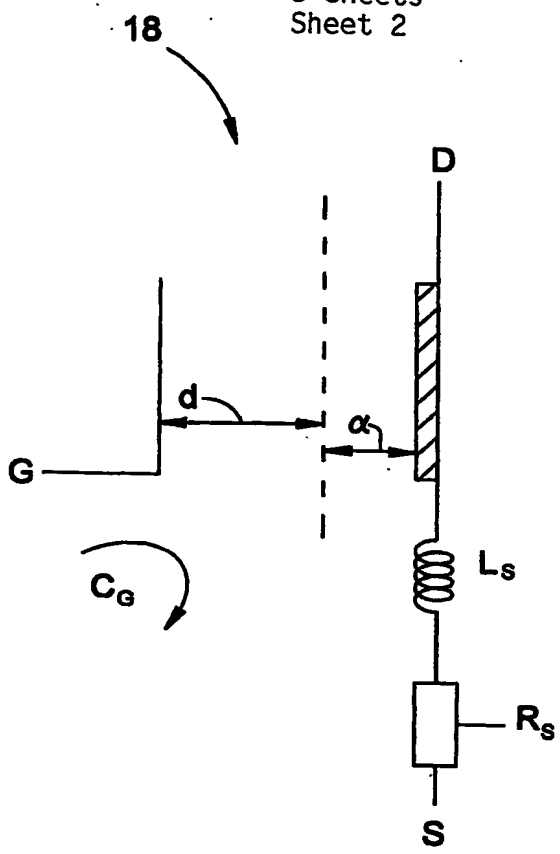

FIGURE 2(b)

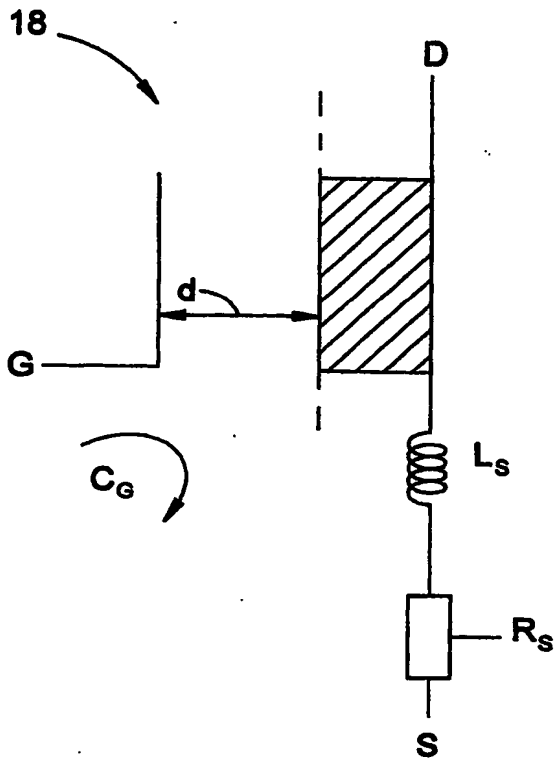

FIGURE 2(c)

D.M. KISCH INC.
Patent Attorneys
JOHANNESBURG

Patent Attorneys for the Applicant

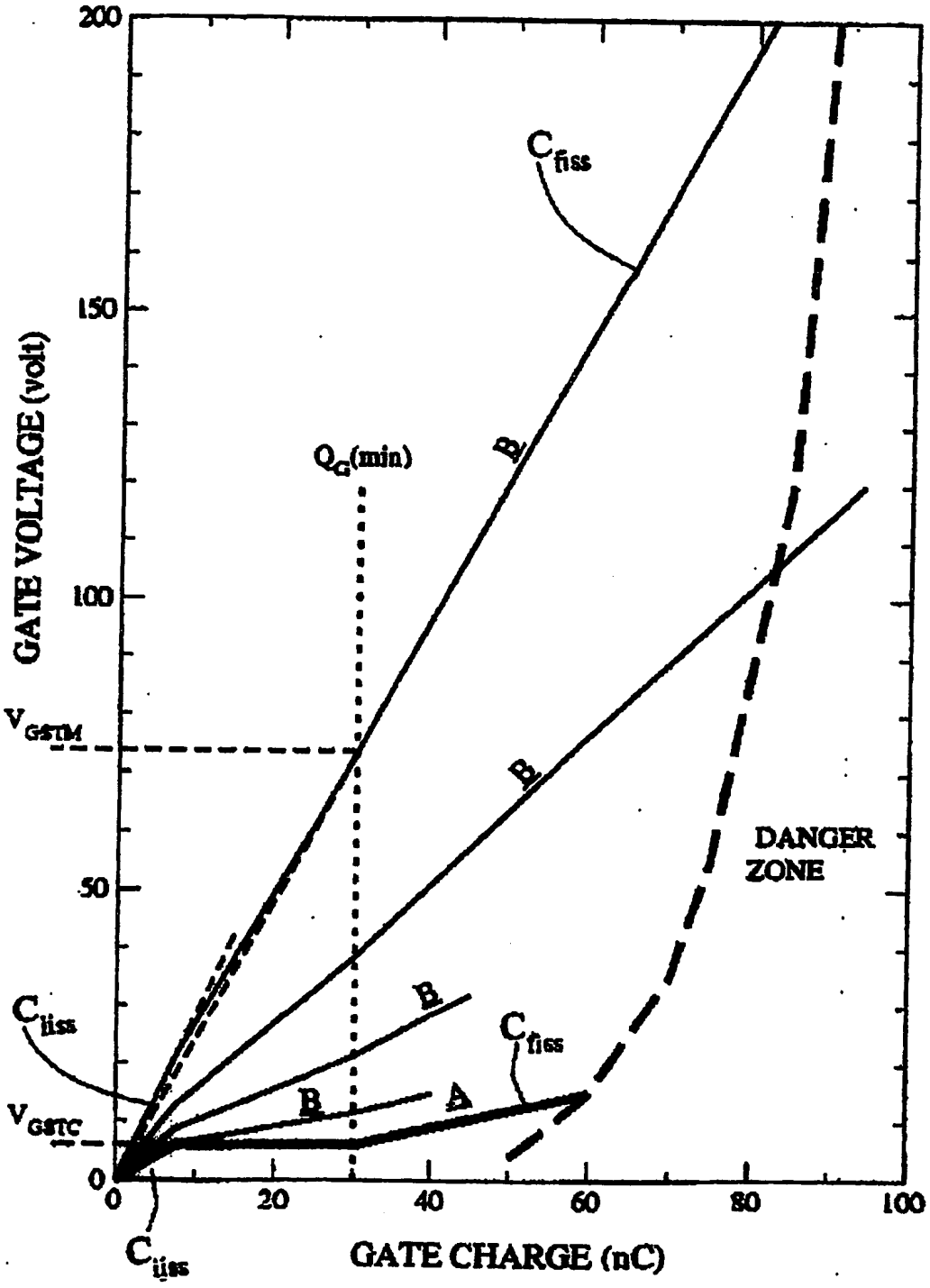

FIGURE 3

D.M. KISCH INC.
Patent Attorneys
JOHANNESBURG

Patent Attorney for the Applicant

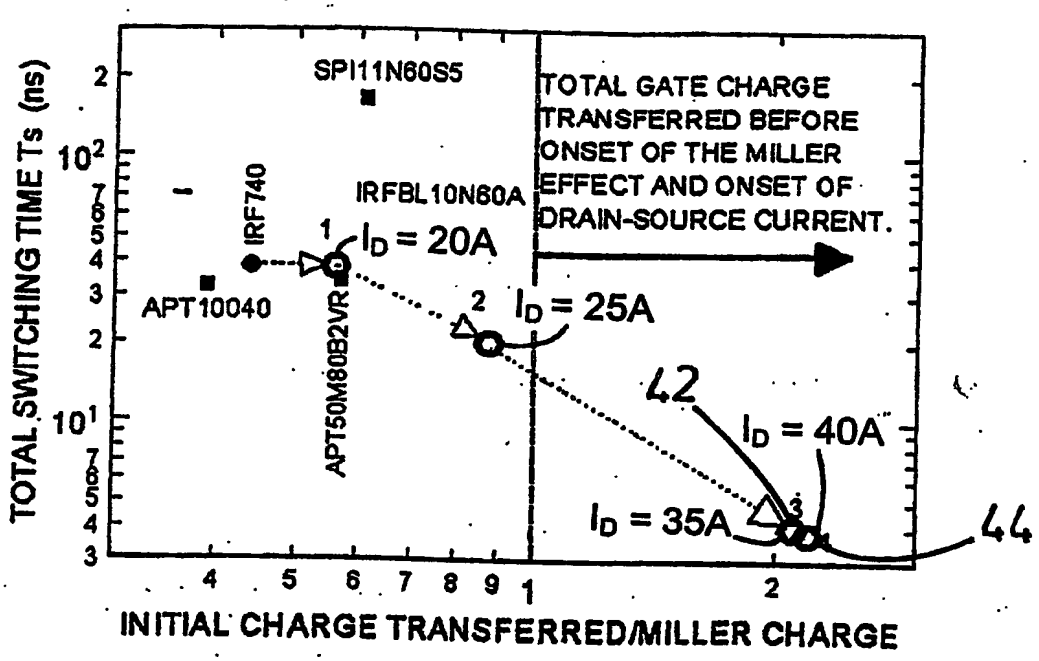

FIGURE 4

D.M. KISCH INC.
Patent Attorneys
JOHANNESBURG

Patent Attorney for the Applicant

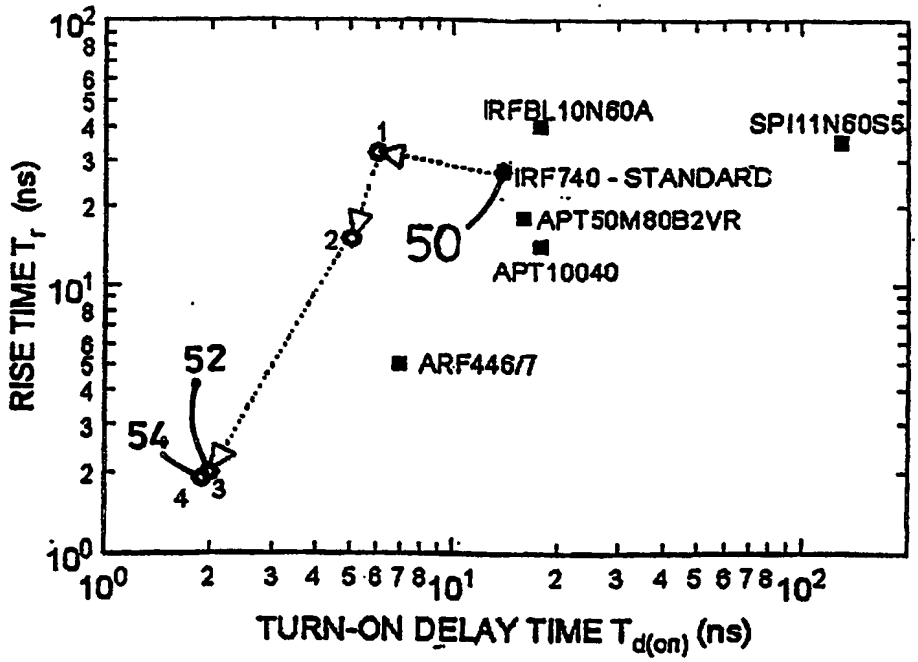

FIGURE 5

D.M. KISCH INC.
Patent Attorneys
JOHANNESBURG

Patent Attorney for the Applicant

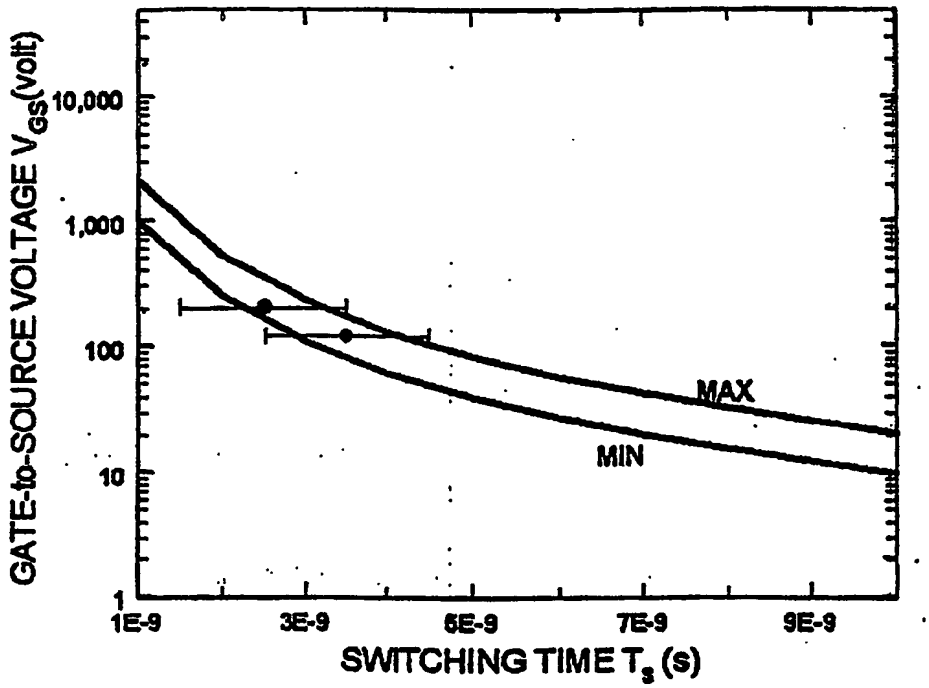

FIGURE 6

D.M. KISCH INC.
Patent Attorneys
JOHANNESBURG

Patent Attorney for the Applicant

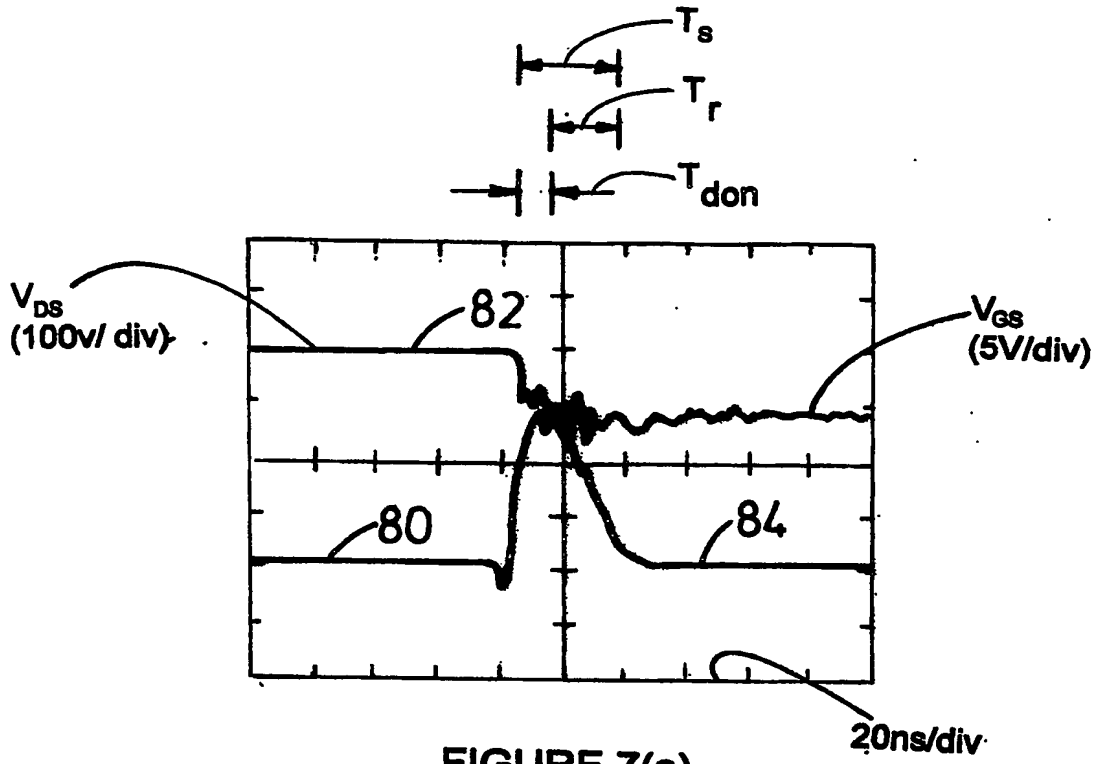

FIGURE 7(a)

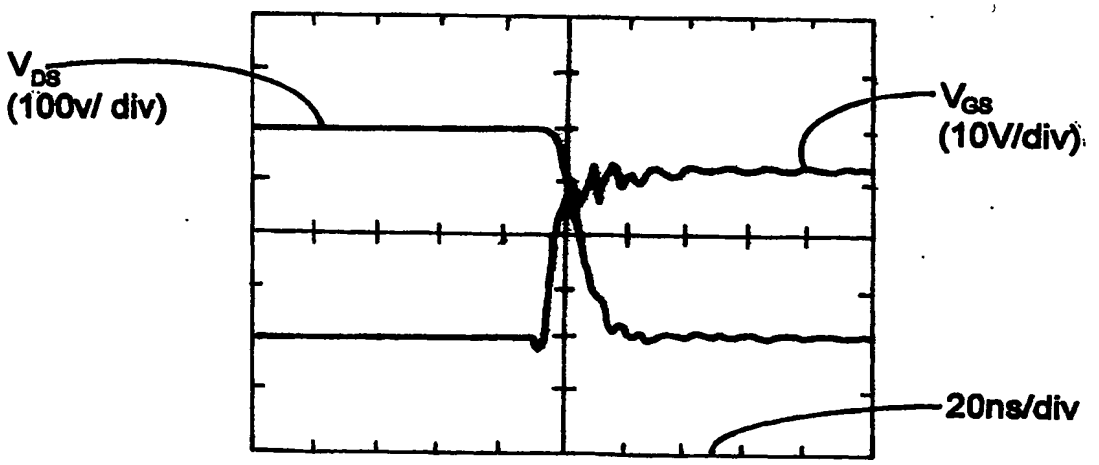

FIGURE 7(b)

D.M. KISCH INC.
Patent Attorneys
JOHANNESBURG

Patent Attorney for the Applicant

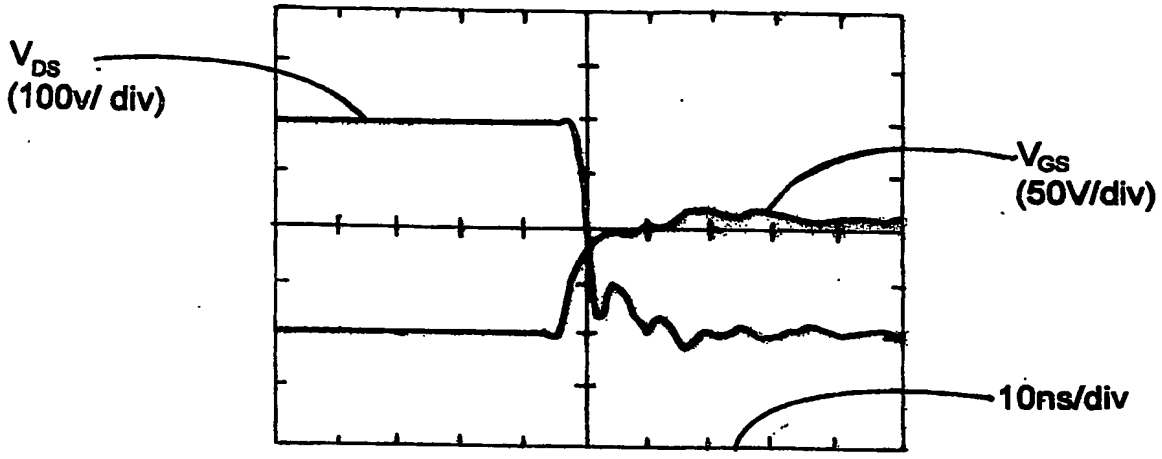

FIGURE 7(c)

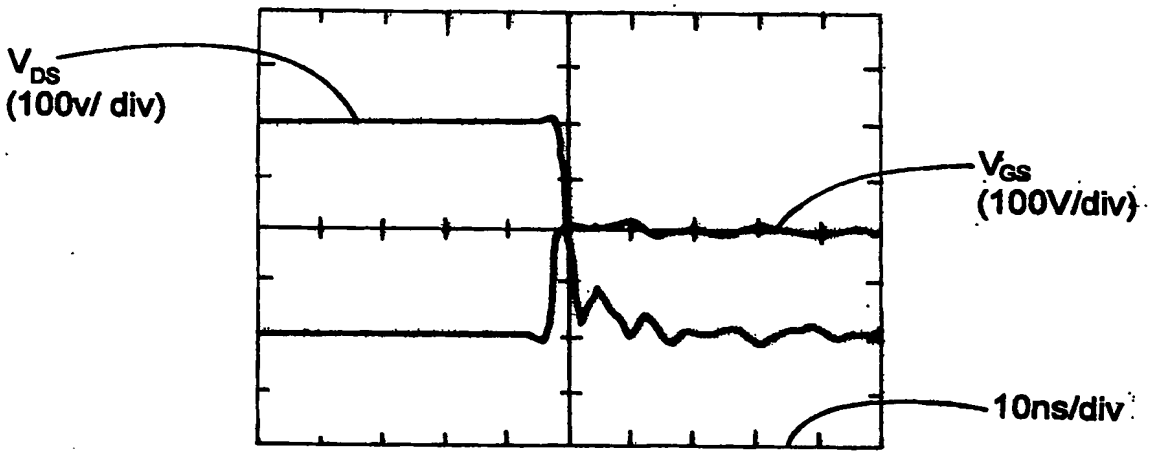

FIGURE 7(d)

D.M. KISCH INC.
Patent Attorneys
JOHANNESBURG

Patent Attorney for the Applicant